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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/696,099 | 10/25/2000 | Richard Douglas Allan | 07703-346001 / WIN0216/J. | 4131 |

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NEW YORK, NY 10111

| EXAMINER |
|---|
| HAMILTON, LALITA M |

| ART UNIT | PAPER NUMBER |
|---|---|
| 3624 | |

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

〜

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 09/696,099 | ALLAN ET AL. |
| | Examiner | Art Unit |
| | Lalita M Hamilton | 3624 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL**.　　2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) _1-25_ is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-25_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a) ☐ All　b) ☐ Some * c) ☐ None of:

　　　1. ☐ Certified copies of the priority documents have been received.

　　　2. ☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _7_.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

# DETAILED ACTION

## *Oath/Declaration*

The oath or declaration is defective. A new oath or declaration in compliance

with 37 CFR 1.67(a) identifying this application by application number and filing date is

required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: It does not identify the citizenship

of each inventor.

## *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly
claiming the subject matter which the applicant regards as his invention.

Claims 7-13 are rejected for the following reasons.

Claims 7, 10, and 12 recite the limitation first-mentioned transaction unit. There

is insufficient antecedent basis for this limitation in the claim.

The remaining claims are rejected for their dependency upon the rejected claims.

## *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

(e) the invention was described in a patent granted on an application for patent by another filed in the
United States before the invention thereof by the applicant for patent, or on an international application
by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this
title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act

of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior

to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Coutts

(6,311,165).

Coutts discloses a transaction processing system and corresponding method

comprising a plurality of transaction units and a controller having a processor and

memory means storing run-time interpreted code units each associated with a

respective transaction unit, the controller being operable to execute the code of each

respective code unit and in response thereto to generate signals controlling the

operation of the respective transaction units (col.3, lines 10-62; col.4, lines 8-35; col.21,

lines 50-63; col.27, line 25 to col.30, line 45; and fig.16-all); a native code unit operable

to accept and process input signals for the purpose of validation of an item of money

(col.13, lines 1-43 and fig.5-all); transaction units are arranged to handle respective

types of payment media (col.4, lines 8-35; col.13, lines 1-43; and fig.5-all); each

interpreted code unit is independently functional without regard to the presence of the

other interpreted code units (col.3, lines 10-62; col.4, lines 8-35; col.21, lines 50-63;

col.27, line 25 to col.30, line 45; and fig.16-all); an API code unit containing routines

which are accessible at run-time by each of the interpreted code modules (col.34, lines

25-31 and col.51, lines 65-67); a memory means is a non-volatile semiconductor

memory (col.18, lines 55-62); a validation code unit operable to accept and process

input signals for the purposes of validation of an item of money, a Java Virtual Machine,

and at least one Java application operable to perform controlling functions for a

respective further transaction unit to which the first mentioned transaction unit is

connected (col.3, lines 10-62; col.4, lines 8-35; col.13, lines 1-43; col.21, lines 50-63;

col.27, line 25 to col.30, line 45; fig.5-all; and fig.16-all); the validation code unit

comprises native code (col.3, lines 10-62; col.4, lines 8-35; col.21, lines 50-63; col.27,

line 25 to col.30, line 45; and fig.16-all); the validation code unit comprises compiled

code (col.3, lines 10-62; col.4, lines 8-35; col.21, lines 50-63; col.27, line 25 to col.30,

line 45; and fig.16-all); a Java application operable to perform controlling functions for

the first mentioned transaction unit (col.3, lines 10-62; col.4, lines 8-35; col.21, lines 50-

63; col.27, line 25 to col.30, line 45; and fig.16-all); the transaction unit is a coin

validation mechanism (col.4, lines 8-35; col.13, lines 1-43; and fig.5-all); at least one

further transaction unit under the control of the microprocessor system in said first-

mentioned transaction unit (col.4, lines 8-35; col.13, lines 1-43; and fig.5-all); the

transaction units are interconnected via a serial link (col.11, line 53 to col.12, line 6); a

plurality of transaction units and a controller having a processor and memory means

storing executable code in respective code modules each associated with a respective

one of the transaction units, the controller being coupled to the transaction units and

arranged to receive and send signals from and to the transaction units, the controller

being operable to execute the code in each respective code module, the code in that

module being functional independently of the code in the other modules and performing

processing operations in response to signals received from its respective transaction

unit indicative of respective operations performed by that transaction unit, and the code

being further operable to cause the controller to generate controlling signals for sending

to the respective transaction unit and capable of representing different functions to be

performed by the transaction unit (col.4, lines 8-35; col.13, lines 1-43; and fig.5-all); the

memory means has executable code in a further code module, that executable code

being responsive to credit-representing signals generated by the code in one or more

modules, being operable to produce vending authorizing signals for use by the

executable code in at least one other module (col.3, lines 10-62; col.4, lines 8-35;

col.13, lines 1-43; col.21, lines 50-63; col.27, line 25 to col.30, line 45; fig.5-all; and

fig.16-all); the executable code is run-time interpreted code (col.3, lines 10-62; col.4,

lines 8-35; col.21, lines 50-63; col.27, line 25 to col.30, line 45; and fig.16-all); the

controller is housed in one of the transaction units (col.3, lines 10-62; col.4, lines 8-35;

col.21, lines 50-63; col.27, line 25 to col.30, line 45; and fig.16-all); each code module is

contained in a respective area of protected memory (col.3, lines 10-62; col.4, lines 8-35;

col.21, lines 50-63; col.27, line 25 to col.30, line 45; and fig.16-all); the executable code

is Java byte code (col.3, lines 10-62; col.4, lines 8-35; col.21, lines 50-63; col.27, line 25

to col.30, line 45; and fig.16-all); the transaction units are interconnected via a serial link

(col.11, line 53 to col.12, line 6); the transaction units include one or more of a coin

mechanism unit  a banknote mechanism unit, a card reader unit, and a vending

machine controller unit (col.13, lines 1-43 and fig.5-all); a controller unit including a

processor operable to execute instructions in Java code, and at least one transaction

unit including means for performing value transactions under the control of the

processor executing code uploaded from the transaction unit (col.13, lines 1-43 and

fig.5-all); the transaction system comprises a plurality of transaction units, and the

controller unit is operable to execute code stored in respective code units each

associated with a respective transaction unit (col.13, lines 1-43 and fig.5-all); the code

units are stored in respective protected memory areas (col.13, lines 1-43 and fig.5-all);

and a method of assembling a transaction system, the transaction system comprising a

plurality of transaction units and a controller having a processor and memory means for

storing executable code in respective code modules each associated with a respective

one of the transaction units, the controller being coupled to the transaction units and

arranged to receive and send signals from and to the transaction units, and the

controller being operable to execute the code in each respective code module, each

code module performing processing operations in response to signals received from the

respective transaction unit indicative of respective operations performed by that

transaction unit, and the code module being further operable to cause the controller to

generate controlling signals for sending to the respective transaction unit and capable of

representing different functions to be performed by the transaction unit; the method

comprising separately loading the executable code for the respective code modules into

the memory means of the controller (col.3, lines 10-62; col.4, lines 8-35; col.13, lines 1-

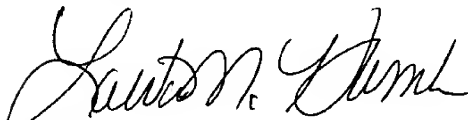43; col.21, lines 50-63; col.27, line 25 to col.30, line 45; fig.5-all; and fig.16-all).

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lalita M Hamilton whose telephone number is (703) 306-5715. The examiner can normally be reached on Tuesday-Thursday (8:30-4:30).

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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